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See HELP NEWS 305.

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03/08/2002

Set	Items	Description
S1	520778	TUNGSTEN OR W OR WOLFRAM
S2	1117520	SILICON OR SI
S3	1751	(SILICON (2N) INSULATOR ( ) METAL ( ) OXID ( ) SEMICONDUCTOR) OR SO-
S4	1584631	I(W) MOSFET OR (SILICON(2N) INSULATOR ( ) METAL (2N) MOSFET)
S5	95617	TRENCH?? OR HOLE? ? OR GROOVE? ? OR CHANNEL? ? OR EDGE? OR
S6	294813	FLUSH OR RIDGE?
S7	184379	(EPI OR EPITAX?) (3N) (LAYER? OR FILM OR FILMS OR COAT?????)
S8	249194	(INSULAT? OR DIELECTRIC OR OXIDE) (3N) (FILM? ? OR LAYER? OR
S9	6481	COAT???? OR OVERCOAT???? OR MATERIAL? OR COVER???? OR MULTILA-
S10	203	YER? OR MULTI(W) LAYER?)
S11	92	GATE? ? OR MEMORY ( ) CELL OR LIBRARY ( ) CELL
S12	44	DRAIN? ? OR DRIFT? ? OR (ACTIVE OR DIFFUSION OR SOURCE) (2N-
S13	22	) (REGION OR REGIONS OR AREAS OR AREA OR ZONE OR ZONES)
S14	15	(BURY??? OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?????) (-
S15	1320	3N) (INSULAT? OR DIELECTRIC OR OXIDE)
S16	176	S3 AND S9
S17	9	S10 AND S8
S18	9	S11 AND S6
		S12 AND S7
		RD (unique items)
		S3 AND (S1 OR S2)
		S15 AND S9
		S15 AND S5
		S17 NOT S14

03/08/2002

? T S14/3, AB/1-5

&gt;&gt;&gt;No matching display code(s) found in file(s): 65

14/3, AB/1 (Item 1 from file: 8)  
 DIALOG(R) File 8: Ei Compendex(R)  
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05535274

E.I. No: EIP00045141734

Title: Behavior of narrow-width SOI MOSFET 's with MESA isolation

Author: Wang, Hongmei; Chan, Mansun; Wang, Yangyuan; Ko, Ping K.

Corporate Source: Peking Univ, Beijing, China

Source: IEEE Transactions on Electron Devices v 47 n 3 2000. p 593-600

Publication Year: 2000

CODEN: IETDAI ISSN: 0018-9383

Language: English

Abstract: Narrow-width effects in thin-film silicon-on-insulator (SOI) MOSFET's with MESA isolation technology have been studied theoretically and experimentally. As the channel width of the MOSFET is scaled down, the gate control of the channel potential is enhanced. It leads to the suppression of drain current dependence on substrate bias and punchthrough effect in narrow-width devices. The variation of threshold voltage with the channel width is also studied and is found to have a strong dependence on thickness of silicon film, interface charges in the buried oxide and channel type of SOI MOSFET. (Author abstract) 20 Refs.

14/3, AB/2 (Item 2 from file: 8)  
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05017096

E.I. No: EIP98054209582

Title: High-current small-parasitic-capacitance MOSFET on a poly-Si interlayered (PSI: Psi) SOI wafer

Author: Horiuchi, Masatada; Teshima, Tatsuya; Tokumasu, Kazuya; Yamaguchi, Ken

Corporate Source: Hitachi Ltd, Tokyo, Jpn

Source: IEEE Transactions on Electron Devices v 45 n 5 May 1998. p 1111-1115

Publication Year: 1998

CODEN: IETDAI ISSN: 0018-9383

Language: English

Abstract: A new type of silicon-on insulator (SOI) structure has been fabricated by using direct bonding technology to bury multilayered films consisting of poly-Si and SiO<sub>2</sub>. A device with an ideal epitaxial channel structure was fabricated using a conventional MOS process on this novel multilayered SOI (100-nm SOI/10-nm SiO<sub>2</sub>/poly-Si/500-nm SiO<sub>2</sub>) wafer. In this device, the highly concentrated p<sup>+</sup> plus poly-Si just beneath the nMOS channel region acts as a punchthrough stopper, and the buried thin back-gate oxide under the SOI layer acts as an impurity diffusion barrier, keeping the impurity concentration in the SOI film at its original low level. The device fabricated was an ultrathin SOI MOSFET capable of operating at a current 1.5 times that of conventional hundred-nm devices at low voltages. (Author abstract) 10 Refs.

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04715971

E.I. No: EIP97063686683  
 Title: 0.18-  $\mu$ m fully-depleted silicon-on-insulator MOSFET's  
 Author: Cao, Min; Kamins, Ted; Voorde, Paul Vande; Diaz, Carlos; Greene, Wayne

Corporate Source: Hewlett-Packard Lab, Palo Alto, CA, USA  
 Source: IEEE Electron Device Letters v 18 n 6 Jun 1997. p 251-253  
 Publication Year: 1997

CODEN: EDLEDZ ISSN: 0741-3106  
 Language: English

Abstract: High-performance 0.18-  $\mu$ m **gate-length** fully-depleted silicon-on-insulator (FD-SOI) **MOSFET's** were fabricated using 4-nm **gate oxide**, 35-nm thick channel, and 80-nm or 150-nm **buried oxide layer**. An elevated source/drain structure was used to provide extra silicon during silicide formation, resulting in low source/drain series resistance. Nominal device drive currents of 560  $\mu$ A/ $\mu$ m and 340  $\mu$ A/ $\mu$ m were achieved for n-channel and p-channel devices, respectively, at a supply voltage of 1.8 V. Improved short-channel performance and reduced self-heating were observed for devices with thinner **buried oxide layers**. (Author abstract) 4 Refs.

14/3,AB/4 (Item 4 from file: 8)  
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04415164

E.I. No: EIP96063202490  
 Title: Comparison of standard and low-dose separation-by-implanted-oxygen substrates for 0.15  $\mu$ m **SOI MOSFET** applications  
 Author: Joachim, Hans-Oliver; Yamaguchi, Yasuo; Fujino, Takeshi; Kato, Takaaki; Inoue, Yasuo; Hirao, Tadashi

Corporate Source: Mitsubishi Electric Corp, Hyogo, Jpn  
 Conference Title: Proceedings of the 1995 International Conference on Solid State Devices and Materials, SSDM'95  
 Conference Location: Osaka, Jpn Conference Date: 19950821-19950824  
 E.I. Conference No.: 44715

Source: Japanese Journal of Applied Physics, Part 1: Regular Papers & Short Notes & Review Papers v 35 n 2B Feb 1996. p 983-987  
 Publication Year: 1996  
 CODEN: JAPNDE

Language: English  
 Abstract: The influence of **buried oxide** thickness on short-channel effects in silicon-on-insulator metal-oxide-semiconductor field-effect transistors (**SOI MOSFET's**) is investigated. It is shown by analytical modeling and numerical simulation that, although a thin **buried oxide** helps to reduce the charge-sharing component of source and drain electric fields through the **oxide layer**, substrate depletion underneath the thin **buried oxide** counteracts the **oxide** thinning. Although this effect is desired below the **source** and **drain regions** to maintain the SOI inherent low junction capacitances, it is detrimental to short-channel-effect suppression. The calculated results are experimentally confirmed on 0.1  $\mu$ m

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m **SOI MOSFET**'s fabricated on both standard and low-dose separation-by-implanted-oxygen (SIMOX) substrates. A new structure for 0.15  $\mu$  m **SOI MOSFET** applications on a thin **buried oxide** substrate is proposed in which substrate depletion below the channel-forming region can be suppressed locally using self-aligned deep ion implantation. (Author abstract) 5 Refs.

14/3,AB/5 (Item 5 from file: 8)  
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02045924

E.I. Monthly No: EI8611108951  
 E.I. Yearly No: EI86045078

Title: ELECTRICAL METHOD TO MEASURE SOI FILM THICKNESSES.  
 Author: Whitfield, Jim; Thomas, Simon

Corporate Source: Motorola Inc, Phoenix, AZ, USA  
 Source: IEEE Electron Device Letters v EDL-7 n 6 Jun 1986 p 347-349

Publication Year: 1986  
 CODEN: EDLEDZ ISSN: 0193-8576

Language: ENGLISH

Abstract: A method to nondestructively measure the silicon film thickness and the **buried insulating film** thickness is presented. The method is based on a silicon-on-insulator (**SOI**) **MOSFET**. Operating in the two regions where the threshold voltage depends on each of the film thicknesses. The method uses a feedback amplifier to hold the **drain** biases nearly constant while the body and/or the buried **gate** voltages are varied. Calculated threshold voltages from the top-**gate** voltages are used to calculate the film thicknesses. The method is illustrated on devices built in oxygen implanted substrates. The electrical measurements compare well with SEM image measurements. 14 refs.  
 ? T S14/3,AB/6-15

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14/3,AB/6 (Item 1 from file: 34)  
 DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
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08049308 Genuine Article#: 241FD Number of References: 18  
 Title: Buried layer engineering to reduce the **drain**-induced barrier lowering of sub-0.05  $\mu$  m **SOI-MOSFET** (ABSTRACT AVAILABLE)

Author(s): Koh R (REPRINT)

Corporate Source: NEC CORP LTD, SILICON SYST RES LABS, 1120 SHIMOKUZAWA/KANAGAWA 2291198//JAPAN/ (REPRINT)

Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1999, V38, N4B (APR), P2294-2299

ISSN: 0021-4922 Publication date: 19990400

Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN

Language: English Document Type: ARTICLE

Abstract: The influence of the buried layer structure on the **drain**-induced barrier lowering (DIBL) is investigated for a silicon-on-insulator metal-oxide-silicon field-effect-transistor (**SOI-MOSFET**) by a two-dimensional device simulator. The buried **layer** thickness and the **dielectric** constant of the buried **layer** are varied systematically. It is found that the degradation on the threshold voltage can be separated into two

components. One component originates from the electric flux via the SOI layer and the other via the **buried layer**. The **buried insulator** engineering which controls the thickness and the **dielectric** constant of the **buried layer** is effective in reducing the latter component. The **gate** length limit can be reduced by 23% by the buried air gap structure where the **dielectric** constant of the **buried layer** is 1.0.

14/3,AB/7 (Item 2 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
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06426994 Genuine Article#: YR906 Number of References: 17  
Title: The influence of the **buried oxide** defects on the **gate** oxide reliability and **drain** leakage currents of the silicon-on-insulator metal-oxide-semiconductor field-effect transistors (ABSTRACT AVAILABLE)  
Author(s): Iwamatsu T (REPRINT) ; Ipposhi T; Yamaguchi Y; Imai Y; Maegawa S ; Tsubouchi N; Nishimura T  
Corporate Source: MITSUBISHI ELECTR CORP,ULSI LAB, 4-1 MIZUHARA/ITAMI/HYOGO 664/JAPAN/ (REPRINT)  
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1997, V36, N12A (DEC), P7104-7109  
ISSN: 0021-4922 Publication date: 19971200  
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN  
Language: English Document Type: ARTICLE  
Abstract: The relation between **gate oxide** and **buried oxide** (BOX) reliabilities was investigated for several silicon on **insulator** (SOI) **materials**. The yield values of the **gate** oxide breakdown depend on the BOX leakage currents. The **gate** leakage currents and BOX leakage currents were observed at the same position by optical luminescence. By scanning electron microscope (SEM) observation at the luminescence region in the low-dose separation by implanted oxygen (SIMOX) substrate, it was found that the SOI layer had disappeared, and voids appeared in the BOX layer. In addition,  $Q_{bd}$  of the **gate** oxide was low in the capacitor where the BOX leakage currents were observed. It is thought that the crystalline quality of the SOI layer on the imperfect BOX layer was degraded, causing the **gate** leakage currents. Moreover, it was observed that the yield value of the **drain** leakage currents of the SOI metal-oxide-semiconductor field-effect transistors (MOSFET's) also depended on the BOX leakage currents.

14/3,AB/8 (Item 3 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
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04736464 Genuine Article#: UD941 Number of References: 5  
Title: COMPARISON OF STANDARD AND LOW-DOSE SEPARATION-BY-IMPLANTED-OXYGEN SUBSTRATES FOR 0.15 MU-M **SOI MOSFET** APPLICATIONS (Abstract Available)  
Author(s): JOACHIM HO; YAMAGUCHI Y; FUJINO T; KATO T; INOUE Y; HIRAO T  
Corporate Source: MITSUBISHI ELECTR CORP,ULSI LAB,4-1 MIZUHARA/ITAMI/HYOGO 664/JAPAN/  
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1996, V35, N2B (FEB), P983-987

ISSN: 0021-4922

Language: ENGLISH Document Type: ARTICLE

Abstract: The influence of **buried oxide** thickness on short-channel effects in silicon-on-insulator metal-oxide-semiconductor field-effect transistors (**SOI MOSFET**'s) is investigated. It is shown by analytical modeling and numerical simulation that, although a thin **buried oxide** helps to reduce the charge-sharing component of source and **drain** electric fields through the **oxide layer**, substrate depletion underneath the thin **buried oxide** counteracts the **oxide** thinning. Although this effect is desired below the **source** and **drain regions** to maintain the SOI inherent low junction capacitances, it is detrimental to short-channel-effect suppression. The calculated results are experimentally confirmed on 0.1  $\mu\text{m}$  **SOI MOSFET**'s fabricated on both standard and low-dose separation-by-implanted-oxygen (SIMOX) substrates. A new structure for 0.15  $\mu\text{m}$  **SOI MOSFET** applications on a thin **buried oxide** substrate is proposed in which substrate depletion below the channel-forming region can be suppressed locally using self-aligned deep ion implantation.

14/3,AB/9 (Item 4 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
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02145313 Genuine Article#: KE569 Number of References: 0  
(NO REFS KEYED)

Title: 2-DIMENSIONAL DEVICE SIMULATION OF 0.1-MU THIN-FILM SOI MOSFETS (Abstract Available)

Author(s): JOACHIM HO; YAMAGUCHI Y; ISHIKAWA K; KOTANI N; NISHIMURA T; TSUKAMOTO K

Corporate Source: MITSUBISHI ELECTR CO,LSI LAB/ITAMI/HYOGO 664/JAPAN/  
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1992, VE75C, N12 (DEC), P 1498-1505

ISSN: 0916-8524

Language: ENGLISH Document Type: ARTICLE

Abstract: Thin- and ultra-thin-film **SOI MOSFET**'s are promising candidates to overcome the constraints for future miniaturized devices. This paper presents simulation results for a 0.1  $\mu\text{m}$  **gate** length **SOI MOSFET** structure using a two-dimensional/two-carrier device simulator with a nonlocal model for the avalanche induced carrier generation. For the suppression of punchthrough effect in devices with a channel doping of  $1 \times 10^{16} \text{ cm}^{-3}$  and 5 nm thick **gate oxide** it is found that the SOI layer thickness has to be reduced to at least 20 nm. The thickness of the **buried oxide** should not be smaller than 50 nm in order to avoid the degradation of thin SOI performance advantages. Investigating ways to suppress the degradation of the subthreshold slope factor at these device dimensions it was found in contrast to the common expectation that the S-factor can be improved by increasing the body doping concentration. This phenomenon, which is a unique feature of thin-film fully depleted **SOI MOSFET**'s, is explained by an analytical model. At lower doping the area of the current flow is reduced by a decreasing effective channel thickness resulting in a slope factor degradation. Other approaches for S-factor improvement are the reduction of the channel edge capacitances by source/**drain** engineering or the decrease of SOI thickness or **gate oxide** thickness. For the latter approach a higher permittivity **gate**

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insulating material should be used in order to prevent tunnelling. The low breakdown voltage can be increased by utilizing an LDD structure to be suitable for a 1.5 V power supply. However, this is at the expense of reduced current drive. An alternative could be the supply voltage reduction to 1.0 V for single drain structure use. A dual-gated SOI MOSFET has an improved performance due to the parallel combination of two MOSFET's in this device. A slightly reduced breakdown voltage indicates a larger drain electric field present in this structure.

14/3,AB/10 (Item 1 from file: 35)  
 DIALOG(R) File 35:Dissertation Abs Online  
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01679301 AAD9913116  
 THIN-FILM SOI MOSFET'S DEVICE PHYSICS, CHARACTERIZATION AND  
 CIRCUIT MODELING (SILICON ON INSULATOR, DYNAMIC DEPLETION APPROACH,  
 CAPACITIVE COUPLING, FLOATING BODY EFFECT)  
 Author: FUNG, KA-HING  
 Degree: PH.D.  
 Year: 1997  
 Corporate Source/Institution: HONG KONG UNIV. OF SCI. AND TECH.  
 (PEOPLE'S REPUBLIC OF CHINA) (1223)  
 Source: VOLUME 59/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.  
 PAGE 5988. 155 PAGES

Silicon-On-Insulator (SOI) technology, which was originally developed for military applications, is finally emerging as a mainstream semiconductor technology. Potential applications such as SRAM, lower power logic and RF IC have been demonstrated by major semiconductor companies. In this thesis, many remaining issues ranging from device physics to circuit modeling have been addressed.

The impacts of silicon film thickness and channel width scaling on Re-oxidized MESA isolation were studied. The subthreshold characteristics and narrow width effect are explained through the geometry of device edge resulted from the sidewall reoxidation.

Several major issues of floating body SOI MOSFET's are addressed in this thesis. The frequency dispersion of output resistance ( $R_{out}$ ) in partially depleted device was studied. The effect is explained by the floating body potential fluctuation under the combined influence of hole accumulation in the neutral body and capacitive coupling. Next, capacitive coupling effect was studied theoretically and experimentally. The body charge model for bulk MOSFET was evaluated for its accuracy in predicting the coupling effect. A simple technique was also proposed to characterize the gate coupling factor.

Lastly, a new compact model suitable for circuit simulation of both Partially Depleted and Fully Depleted SOI MOSFET's was developed. A *Dynamic Depletion Approach* is proposed to model the automatic transition between different depletion modes. Though the joint effort of the graduate researchers in University of California at Berkeley and our group, the model has been installed into Berkeley SPICE 3f4 as BSIM3SOI. Charges and drain current are scaleable with buried oxide and silicon film thickness. Most of the SOI specific effects such as self-heating, parasitic bipolar, non-ideal body contact and backgate effect are included. The C-V model is improved for better accuracy in capacitive coupling prediction. The model is now under evaluation by many companies and SEMATECH.



03/08/2002

14/3,AB/11 (Item 2 from file: 35)  
 DIALOG(R)File 35:Dissertation Abs Online  
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01487617 AADAAI9618678

INVESTIGATION OF INTERFACE PROPERTIES AND HOT CARRIER DEGRADATION EFFECTS  
 IN SILICON-ON-INSULATOR MATERIALS AND DEVICES (MOSFET)

Author: CHANG, YUN-SHAN

Degree: PH.D.

Year: 1995

Corporate Source/Institution: UNIVERSITY OF FLORIDA (0070)

Source: VOLUME 57/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 1302. 161 PAGES

This research effort mainly deals with the studies of interface properties and parasitic bipolar conduction on hot carrier degradation effects and the modeling of the GAA (Gate-All-Around) MOSFET's in thin-film silicon-on-insulator (SOI) materials and devices. It consists of three parts: In the first part, a contactless S-polarized reflectance optical technique for mapping and determining the top Si film and buried oxide layer thicknesses and an optical modulation technique for determining and mapping the interface recombination velocities and substrate carrier lifetimes in SIMOX (Separation by Implantation of OXYgen) SOI wafers have been developed for use as quality control and processing evaluation tools in the fabrication of ULSI circuits. In the second part, the extraction of degradation parameters in the defective region after hot carrier stress and the modeling of floating body effects in the partially depleted (PD) SOI devices are presented. In the third part, A modeling of GAA devices and the extraction of parameters are depicted.

Mapping of the top Si film and buried oxide thicknesses in a SIMOX wafer was performed by using a contactless S-polarized reflectance optical modulation (DBSPR) technique. The DBSPR method is based on the S-polarized reflectance measured at oblique incident angles in the SIMOX wafer. A theoretical model was developed to extract the top Si film and buried oxide layer thicknesses from the DBSPR technique. Mapping of the interface recombination velocities and substrate carrier lifetimes in a SIMOX wafer was performed by using a contactless optical modulation technique. The optical method is based on the modulation of transmission intensity of an infrared (IR) probe-beam by a visible pump-beam ( $h\nu \geq E_g$ ) via free carrier absorption in the SIMOX wafer. A theoretical model was developed to determine the interface recombination velocities and substrate carrier lifetimes from the optical modulation technique. The evaluation of implantation-condition effects on the defect formation mechanisms in an annealed SIMOX wafer by using the DBSPR and the optical modulation techniques is also presented.

The extraction of degradation parameters in the defective region after hot carrier stress in the PD SOI MOSFET's is discussed. Moreover, the developed model and the experimental results reveal the aggravation of hot carrier effects on the parasitic bipolar transistor conduction in the PD SOI devices. Using the two-piece model, the degradation parameters in the defective region can be extracted. The modification of kink behavior, breakdown voltage, and parasitic bipolar action after the hot carrier stress is predicted by the developed models and observed in the experiment.

Modeling of the GAA devices was developed. The gate-all-around structure of the GAA devices provides the enhancement of drain current and transconductance. Due to the volume-inversion effect, the

mobility is enhanced in the GAA devices. Using the measured **drain** current versus **gate** voltage characteristics, the modeling parameters can be obtained. Several current-voltage methods are employed to verify the extracted parameters.

14/3,AB/12 (Item 3 from file: 35)  
DIALOG(R)File 35:Dissertation Abs Online  
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01400125 AAD9505658  
DEVELOPMENT OF NEW CHARACTERIZATION TECHNIQUES FOR THIN-FILM  
SILICON-ON-INSULATOR (SOI) MATERIALS AND DEVICES (THIN FILMS)  
Author: YANG, PING-CHANG  
Degree: PH.D.  
Year: 1993  
Corporate Source/Institution: THE UNIVERSITY OF FLORIDA (0070)  
Source: VOLUME 55/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.  
PAGE 4539. 132 PAGES

This research effort mainly deals with the development of new electrical and optical characterization techniques and the modeling of thin-film silicon-on-insulator (SOI) materials and devices for VLSI applications. It consists of three parts: In the first part, a contactless optical technique for mapping and determination of film and substrate carrier lifetimes in SIMOX (Separation by IMplantation of OXygen) SOI wafers has been developed for evaluating the quality of incoming wafer lots to avoid fabricating VLSI circuits on poor quality SOI materials. In the second part, two electrical characterization techniques using test structures of thick- and thin-film SOI MOSFETs for determining the interface properties of the SOI devices are presented. In the third part, analysis of current-voltage characteristics and extraction of small-signal parameters for fully depleted SOI MOSFETs are discussed.

Mapping of the film and substrate carrier lifetimes in a SIMOX wafer has been carried out by using a contactless dual beam optical modulation (DBOM) technique. The DBOM method is based on the modulation of transmission intensity of an infrared (IR) probe-beam by a visible pump-beam ( $h\nu_{\text{ge}} \{ \text{E} \}_{\text{sb}} \{ \text{g} \}$ ) via free carrier absorption in the SIMOX wafer. A theoretical model has been developed to extract the excess carrier lifetimes from the DBOM technique.

The modified High-Low-Frequency (HLF) transconductance method is applied to characterize the properties of film/front-**gate-oxide** and film/**buried-oxide** interfaces of partially and fully depleted SOI MOSFETs operating in linear region. A new threshold voltage method is developed for characterizing the interface state densities profile in thin (fully depleted) film SOI MOSFETs. This technique is particularly attractive since it requires only simple static **drain** current measurements.

The current-voltage characteristics for a fully depleted SOI MOSFET is analyzed by relating the inversion charge density to the front surface potential from the theories developed for bulk Si and SOI MOSFETs. The analysis, which is valid for back surface depletion and accumulation, gives correctly the threshold voltage, the **drain** current, and the transconductance in all regions of operation. The charge-sheet model and strong-inversion assumption are used in this analysis. Based on the current-voltage characteristics and charge-neutrality relation, small-signal parameters for a thin-film SOI MOSFET are extracted.

14/3,AB/13 (Item 1 from file: 94)  
DIALOG(R)File 94:JICST-EPlus  
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01738745 JICST ACCESSION NUMBER: 93A0120343 FILE SEGMENT: JICST-E  
Special Issue on SOI(Si on Insulator) Devices. Two-Dimensional Device  
Simulation of 0.1.MU.m Thin-Film **SOI MOSFET's**.  
JOACHIM H-O (1); YAMAGUCHI Y (1); ISHIKAWA K (1); KOTANI N (1); NISHIMURA T  
(1); TSUKAMOTO K (1)  
(1) Mitsubishi Electric Corp., Itami-shi, JPN  
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1992, VOL.E75-C,NO.12,  
PAGE.1498-1505, FIG.15, REF.22  
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524  
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3  
LANGUAGE: English COUNTRY OF PUBLICATION: Japan  
DOCUMENT TYPE: Journal  
ARTICLE TYPE: Original paper  
MEDIA TYPE: Printed Publication  
ABSTRACT: Thin- and ultra-thin-film **SOI MOSFET's** are promising  
candidates to overcome the constraints for future miniaturized devices.  
This paper presents simulation results for a 0.1.MU.m **gate** length  
**SOI MOSFET** structure using a two-dimensional/two-carrier  
device simulator with a nonlocal model for the avalanche induced  
carrier generation. For the suppression of punchthrough effect in  
devices with a channel doping of  $1 \times 10^{16} \text{cm}^{-3}$  and 5nm thick **gate**  
oxide it is found that the SOI layer thickness has to be reduced to at  
least 20nm. The thickness of the **buried oxide** should not be  
smaller than 50nm in order to avoid the degradation of thin SOI  
performance advantages. Investigating ways to suppress the degradation  
of the subthreshold slope factor at these device dimensions it was  
found in contrast to the common expectation that the S-factor can be  
improved by increasing the body doping concentration. This phenomenon,  
which is a unique feature of thin-film fully depleted **SOI**  
**MOSFET'S**, is explained by an analytical model. At lower doping  
the area of the current flow is reduced by a decreasing effective  
channel thickness resulting in a slope factor degradation. Other  
approaches for S-factor improvement are the reduction of the channel  
edge capacitances by source/**drain** engineering or the decrease of  
SOI thickness or **gate** oxide thickness. For the latter approach a  
higher permittivity **gate insulating material** should  
be used in order to prevent tunnelling. The low breakdown voltage can  
be increased by utilizing an LDD structure to be suitable for a 1.5V  
power supply. However, this is at the expense of reduced current drive.  
An alternative could be the supply voltage reduction to 1.0V for single  
**drain** structure use. A dual-**gated SOI MOSFET**  
has an improved performance due to the parallel combination of two  
MOSFET's in this device. A slightly reduced breakdown voltage indicates  
a larger **drain** electric field present in this structure. (author  
abst.)

14/3,AB/14 (Item 1 from file: 144)  
DIALOG(R)File 144:Pascal  
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13541814 PASCAL No.: 98-0242629  
High-current small-parasitic-capacitance MOSFET on a poly-Si interlayered  
(PSI:&PSgr;) SOI wafer

HORIUCHI M; TESHIMA T; TOKUMASU K; YAMAGUCHI K

Hitachi Ltd, Tokyo, Japan

Journal: IEEE Transactions on Electron Devices, 1998, 45 (5) 1111-1115

Language: English

A new type of silicon-on insulator (SOI) structure has been fabricated by using direct bonding technology to bury multilayered films consisting of poly-Si and SiO<sub>2</sub>. A device with an ideal epitaxial channel structure was fabricated using a conventional MOS process on this novel multilayered SOI (100-nm SOI/10-nm SiO<sub>2</sub>/poly-Si/500-nm SiO<sub>2</sub>) wafer. In this device, the highly concentrated p<sup>+</sup> SUP & plus; poly-Si just beneath the nMOS channel region acts as a punchthrough stopper, and the **buried thin back-gate oxide** under the SOI **layer** acts as an impurity diffusion barrier, keeping the impurity concentration in the SOI film at its original low level. The device fabricated was an ultrathin **SOI MOSFET** capable of operating at a current 1.5 times that of conventional hundred-nm devices at low voltages.

14/3,AB/15 (Item 2 from file: 144)

DIALOG(R) File 144:Pascal

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12046443 PASCAL No.: 95-0242380

Numerical prediction for 2 GHz RF amplifier of SOI power MOSFET

Solid state devices and materials

OMURA I; NAKAGAWA A

TARUCHA SEIGO, ed; ARAKAWA YASUHIKO, ed; FUKUMA MASAO, ed; FURUYA

KAZUHITO, ed; HORIKOSHI YOSHIJI, ed; IMAI HAJIME, ed; ISHIWARA HIROSHI, ed;

KARAYAMA YOSHIFUMI, ed; MIYAO MASANOBU, ed; NAKASHIMA HISAO, ed; SHIRAKI

YASUHIRO, ed; SUSAKI WATARU, ed; YOSHIMI MAKOTO, ed

Toshiba Corp., res. development cent., Saiwai-ku Kawasaki 210, Japan

Japan Society of Applied Physics, Tokyo, Japan.

SSDM'94. International conference (Yokohama, Kanagawa JPN) 1994-08-23

Journal: Japanese journal of applied physics, 1995, 34 (2B p.1) 827-830

Language: English

RF performance of a metal-oxide-semiconductor field effect transistor (MOSFET) on silicon-on-insulator (SOI) with 0.5  $\mu\text{m}$  **gate** length and 2  $\mu\text{m}$  **buried oxide** thickness has been numerically predicted using a 2-D device simulator to check its applicability to digital cellular telephones. The device has been found to have excellent performance for a 2 GHz high-power amplifier at a power supply of 2.8 V. The calculated cutoff frequency and maximum frequency of oscillation for the intrinsic MOSFET are 23 GHz and 65 GHz, respectively. The **SOI MOSFET** is a promising candidate for replacing GaAs MESFETs in 2 GHz RF applications

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Serial No.:09/924,787

? T S18/3,AB/1-9

>>>No matching display code(s) found in file(s): 65

18/3,AB/1 (Item 1 from file: 8)  
DIALOG(R)File 8: Ei Compendex(R)  
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04464719

E.I. No: EIP96083273072  
Title: Ultra-thin, highly uniform thin film **SOI MOSFET** with low series resistance using pattern-constrained epitaxy (PACE)  
Author: Wong, H.-S.; Chan, K.; Lee, Y.; Roper, P.; Taur, Y.  
Corporate Source: I.B.M. Thomas J. Watson Research Cent, Yorktown Heights, NY, USA  
Conference Title: Proceedings of the 1996 Symposium on VLSI Technology  
Conference Location: Honolulu, HI, USA Conference Date: 19960611-19960613  
E.I. Conference No.: 45102  
Source: Digest of Technical Papers - Symposium on VLSI Technology 1996. IEEE, Piscataway, NJ, USA, 96CH35944. p 94-95  
Publication Year: 1996  
CODEN: DTPTEW ISSN: 0743-1562  
Language: English

Abstract: We report a novel fabrication process for a self-aligned, ultra-thin, highly uniform thin film **SOI MOSFET** with low series resistance. SOI films as thin as 11 nm with 5% uniformity across the wafer was achieved. Self-aligned, ultra-thin SOI n-MOSFET's with 8 nm- 50 nm undoped channel were fabricated. Excellent device characteristics ( $L_{eff}$  equals 0.2  $\mu$ m,  $g_m$  equals 242 mS/mm,  $R_{ds(on)}$  equals 333  $\Omega$  -  $\mu$ m,  $A_{eff}/(g_m/g_{ds})$  equals 43) were obtained. (Author abstract) 10 Refs.

18/3,AB/2 (Item 2 from file: 8)  
DIALOG(R)File 8: Ei Compendex(R)  
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03347006

E.I. Monthly No: EI9112157681  
Title: An analytical model for snapback in n-channel **SOI MOSFET's**.  
Author: Huang, J. S. T.; Kueng, Jeffrey S.; Fabian, Terry  
Corporate Source: Honeywell, Inc, Plymouth, MN, USA  
Source: IEEE Transactions on Electron Devices v 38 n 9 Sep 1991 p 2082-2091  
Publication Year: 1991  
CODEN: IETDAI ISSN: 0018-9383  
Language: English

Abstract: An analytical snapback model for n-channel **silicon** -on-insulator (SOI) transistors with body either tied to the source or floating is been presented. The snapback is modeled as a nonlinear feedback system leading to negative transconductances from which the jump in current can occur at the point of instability. The crux of this model is based on the strong dependence of the transistor threshold voltage on the body potential when the body potential is above the transistor surface potential at strong inversion. No parasitic bipolar action is invoked to account for the snapback phenomena. The model correctly predicts the occurrence of hysteresis/latch phenomena and the conditions under which the current jump occurs despite some gross approximations in the electric field and the

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injection level. Results obtained from this model show good agreement with experimental data measured from SIMOX devices fabricated on 0.3-  $\mu$  m epi film. 6 Refs.

18/3, AB/3 (Item 3 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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01913618

E.I. Monthly No: EIM8512-079901  
Title: 3-DIMENSIONAL INTEGRATION FABRICATED BY USING SEEDED LATERAL EPITAXIAL FILM ON SiO<sub>2</sub>.  
Author: Sasaki, N.; Iwai, T.; Kawamura, S.; Mukai, R.; Wada, K.; Nakano, M.

Corporate Source: Fujitsu Ltd, IC Development Div, Kawasaki, Jpn  
Conference Title: Comparison of Thin Film Transistor and SOI Technologies. (Part of the Materials Research Society Spring Meeting.)  
Conference Location: Albuquerque, NM, USA Conference Date: 19840226  
E.I. Conference No.: 06203  
Source: Materials Research Society Symposia Proceedings v 33. Publ by North-Holland, New York, NY, USA and Amsterdam, Neth p 149-154  
Publication Year: 1984  
CODEN: MRSPDH ISSN: 0272-9172 ISBN: 0-444-00899-3  
Language: English

Abstract: Seeded lateral epitaxial laser-recrystallization of silicon film on SiO<sub>2</sub> is applied to fabricate 3-dimensional (3-D) integrations: 3-D CMOS 7-stage ring oscillators. Top p-channel Si-gate SOI MOSFET's are fabricated in the seeded recrystallized silicon directly above bottom n-channel Si-gate bulk MOSFET's with insulator in between. The recrystallized silicon at the seed region can be utilized for buried contact to interconnect bottom and top MOSFET's. At the arsenic implantation step to fabricate source and drain of the bottom MOSFET's, ions are not implanted into the seed region to prevent heavy doping and crystal disorder there; otherwise the dopant diffuses laterally and residual crystal disorder disturbs the epitaxial recrystallization. After the laser-recrystallization, the seed region is implanted with phosphorus to interconnect the top and bottom MOSFET's. 11 refs.

18/3, AB/4 (Item 4 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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01878673

E.I. Monthly No: EIM8507-036773  
Title: LOW TEMPERATURE FABRICATION OF SOI-MOSFET'S IN Si/CaF<sub>2</sub>/Si HETEROEPITAXIAL STRUCTURES.  
Author: Asano, Tanemasa; Wakabayashi, Shinichi; Ishiwara, Hiroshi  
Corporate Source: Tokyo Inst of Technology, Graduate Sch of Science & Engineering, Yokohama, Jpn  
Conference Title: 16th (1984 International) Conference on Solid State Devices and Materials.  
Conference Location: Kobe, Jpn Conference Date: 19840830  
E.I. Conference No.: 05680  
Source: Conference on Solid State Devices and Materials 16th. Publ by Business Cent for Academic Soc Japan, Tokyo, Jpn p 519-522  
Publication Year: 1984

03/08/2002

Serial No.:09/924,787

CODEN: EACMES ISBN: 4-930813-07-7

Language: English

Abstract: The **epitaxial** growth of **Si** films on **CaF//2/**  
**Si** heteroepitaxial structures and characteristics of MOSFET's  
fabricated in the **Si/CaF//2/Si** structures are investigated.  
Both the growth of the **Si/CaF//2/Si** structures and the  
fabrication of MOSFET's are performed at temperatures below 800 DEGREE C.  
For the growth of **Si** films, a new growth method, which involves in  
situ deposition of a thin ( LESS THAN EQUIVALENT TO 10nm) **Si** onto the  
**CaF//2** surface at room temperature prior to deposition of **Si** at  
elevated temperatures, has been developed in order to prevent interfacial  
reaction between deposited **Si** and underlying **CaF//2**. Al gate  
n-channel MOSFET's, which are electrically isolated from the substrates,  
have been fabricated by utilizing plasma enhanced CVD **SiO//2** as the gate  
insulator. The maximum field effect mobility of about 180 cm\*\*2/V X (TIMES)  
s has been obtained. 8 refs.

18/3,AB/5 (Item 5 from file: 8)  
DIALOG(R)File 8:EI Compendex(R)  
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01779509

E.I. Monthly No: EI8507060182

E.I. Yearly No: EI85101879

Title: SIMULATION OF DEEP DEPLETED **SOI MOSFET'S** WITH BACK  
POTENTIAL CONTROL.

Author: Balestra, Francis; Brini, Jean; Gentil, Pierre

Corporate Source: CNRS, Lab de Physique des Composants & Semiconducteurs,  
Grenoble, Fr

Source: Physica B: Physics of Condensed Matter & C: Atomic, Molecular and  
Plasma Physics, Optics v 129 B-C n 1-3 Mar 1985, Solid State Devices 1984,  
Proc of the 14th Eur Solid State Device Res Conf, Incl Solid State Device  
Technol, Lille, Fr, Sep 10-13 1984 p 296-300

Publication Year: 1985

CODEN: PHBCDQ ISSN: 0165-1757

Language: ENGLISH

Abstract: The authors consider **SOI MOSFET** structures of N and  
P types for which a control of the back potential of the **epi**  
**layer** is obtained by using a back gate. The action of the interface  
parameters on the back and front threshold voltages is analyzed in the case  
of a strong coupling between the front and back interface (lightly doped  
**epi layer**). This analysis is carried out by a numerical  
simulation of Poisson's equation throughout the structure. They thus obtain  
the potential profile and the electron and hole densities, as a function of  
front (V//g//1) and back (V//g//2) gate voltages. 6 refs.

18/3,AB/6 (Item 1 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
(c) 2002 Inst for Sci Info. All rts. reserv.

06736109 Genuine Article#: ZN627 Number of References: 12

Title: **Epitaxial Si** on **Al2O3** films grown with O-2 gas by  
the ultrahigh-vacuum chemical vapor deposition method (ABSTRACT  
AVAILABLE)

Author(s): Kimura T (REPRINT) ; Yaginuma H; Sengoku A; Moriyasu Y; Ishida M

Corporate Source: TOYOHASHI UNIV TECHNOL,DEPT ELECT & ELECT ENGN, TEMPAKU  
CHO/TOYOHASHI/AICHI 441/JAPAN/ (REPRINT)

03/08/2002

Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT  
NOTES & REVIEW PAPERS, 1998, V37, N3B (MAR), P1285-1288

ISSN: 0021-4922 Publication date: 19980300

Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI  
4-CHOME, MINATO-KU TOKYO 105, JAPAN

Language: English Document Type: ARTICLE

Abstract: By an improved Al<sub>2</sub>O<sub>3</sub> (100) growth on Si(100) using O-2 gas instead of N<sub>2</sub>O gas, high-crystalline quality silicon on insulates (SOI) and multistacked SOI structures were successfully fabricated on a 2-inch Si(100) wafer by the ultrahigh-vacuum chemical vapor deposition (UHV-CVD) method. The surface morphology of the Si top layer of the fabricated SOI structure is better than that of the silicon on sapphire (SOS) structure grown by the UHV-CVD method. The transistor action was confirmed from the electrical properties of the MOSFET, and the field effect mobility of 748 cm<sup>2</sup>/V s was obtained. These results were similar to those obtained from bulk Si. This improved Si top layer of SOI and multistacked SOI structures is due to the improved surface morphology and crystalline quality of the Al<sub>2</sub>O<sub>3</sub> layer grown on Si with O-2 gas.

18/3,AB/7 (Item 2 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
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06621492 Genuine Article#: ZF327 Number of References: 10  
Title: Vertical MOSFET with buried gate (ABSTRACT AVAILABLE)

Author(s): Kodama M (REPRINT) ; Uesugi T; Mitsushima Y; Taga Y  
Corporate Source: TOYOTA CENT RES & DEV LABS INC,/AICHI 48011//JAPAN/

(REPRINT)  
Journal: ELECTRONICS AND COMMUNICATIONS IN JAPAN PART II-ELECTRONICS, 1997  
, V80, N9 (SEP), P19-25

ISSN: 8756-663X Publication date: 19970900

Publisher: SCRIPTA TECHNICA-JOHN WILEY & SONS, 605 THIRD AVE, NEW YORK, NY  
10158

Language: English Document Type: ARTICLE

Abstract: The authors are investigating an SPE method, using the low-pressure chemical vapor deposition (LPCVD) system, that is utilized in ordinary Si LSI processes. A vertical MOSFET with a unique structure was devised by applying this method. The device assumes a vertical power MOSFET and features in the buried gate. By driving the buried gate in parallel with the ordinary gate, the drain current is increased. This is due to two effects. First, the effect of the channel formed by the buried gate. Second, the effect of the storage layer formed in the low-density n region below the buried gate, which attracts the drain current uniformly. A lateral SOI MOSFET is constructed and is evaluated on the same Si substrate as the vertical MOSFET. The purpose is to evaluate the circuit elements for an intelligent power MOS. The MOS operation is verified for both nMOS and pMOS. The off-state leak current is less than  $2 \times 10^{-12}$  A. (C) 1998 Scripta Technica.

18/3,AB/8 (Item 3 from file: 34)  
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
(c) 2002 Inst for Sci Info. All rts. reserv.

06590056 Genuine Article#: ZD214 Number of References: 21  
Title: Full-band Monte Carlo investigation of hot carrier trends in the



scaling of metal-oxide-semiconductor field-effect transistors ( ABSTRACT AVAILABLE)

Author(s): Duncan A (REPRINT) ; Ravaioli U; Jakumeit J  
Corporate Source: INTEL CORP, /HILLSBORO//OR/97124 (REPRINT); UNIV ILLINOIS, BECKMAN INST, COORDINATED SCI LAB/URBANA//IL/61801; UNIV COLOGNE, INST PHYS 2/D-50937 COLOGNE//GERMANY/  
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1998, V45, N4 (APR), P 867-876

ISSN: 0018-9383 Publication date: 19980400

Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394

Language: English Document Type: ARTICLE

Abstract: A full-band Monte Carlo (MC) device simulator has been used to study the effects of device scaling on hot electrons in different types of n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) structures. Simulated devices include a conventional MOSFET with a single source/drain implant, a lightly-doped drain (LDD) MOSFET, a silicon-on-insulator (SOI) MOSFET, and a MOSFET built on an **epitaxial layer** on top of a heavily-doped ground plane. Different scaling techniques have been applied to the devices, to analyze the effects on the electric field and on the energy distributions of the electrons, as well as on drain, substrate, and gate currents. The results provide a physical basis for understanding the overall behavior of impact ionization and gate oxide injection and how they relate to scaling. The observed nonlocality of transport phenomena and the nontrivial relationship between electric fields and transport parameters indicate that simpler models cannot adequately predict hot carrier behavior at the channel lengths studied (sub-0.3- $\mu$ m). In addition, our results suggest that below 0.15  $\mu$ m, the established device configurations (e.g., LDD) that are successful at suppressing the hot carrier population for longer channel lengths, become less useful and their cost-effectiveness for future circuit applications needs to be reevaluated.

18/3,AB/9 (Item 1 from file: 144)  
DIALOG(R) File 144:Pascal  
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14812518 PASCAL No.: 00-0494805  
Growth of epitaxial CoSi SUB 2 for contacts of ultra-thin SOI MOSFETs  
Proceedings of the International Joint Conference on **Silicon**  
Epitaxy and Heterostructures (IJC-Si), 12-17 September, 1999, Miyagi, Japan

SAKAMOTO K; MAEDA T; HASEGAWA M  
SHIRAKI Yasuhiro, ed; ZAIMA Shigeaki, ed; MIYAO Masanobu, ed; YASUDA Yukio, ed; MUROTA Junichi, ed

Electrotechnical Laboratory, 1-1-4 Umezono, Tsukuba, 305-8568, Japan  
The University of Tokyo, Japan; Nagoya University, Japan; Kyushu University, Japan; Tohoku University, Japan

Japan Society for the Promotion of Science, Japan; Tohoku University.  
Research Institute of Electrical Communication, Japan

International Joint Conference on Silicon Epitaxy and Heterostructures (IJC-Si) International Symposium on Silicon Molecular Beam Epitaxy (Si-MBE), 8 International Symposium on Silicon Heterostructures: From Physics to Devices (Si-HS), 3 (Miyagi JPN) 1999-09-12

Journal: Thin solid films, 2000, 369 (1-2) 240-243

Language: English

Epitaxial CoSi SUB 2 growth for source/drain contacts of a ultra-thin

03/08/2002

Serial No.:09/924,787

silicon on insulator (SOI) MOSFET is discussed. In order to attain low series resistance, heavily doped Si diffusion layer should be left undepleted under the grown CoSi SUB 2. Contact resistance between epitaxial CoSi SUB 2 and n SUP + Si(001) increases when less than 1 nm Co is deposited. A salicide compatible process, forming a thin epitaxial CoSi SUB 2 template by oxide mediated epitaxy followed by reaction deposition epitaxy to increase thickness, is effective in growing CoSi SUB 2 epitaxially up to a few tens of nm.